

U.S. Application Serial No. 09/591,682

### REMARKS

The present amendment is in response to the Official Action dated May 21, 2003, wherein the Examiner rejected pending claims 1-16 and 29-34. More specifically, claims 1-14 are rejected as being anticipated by Heath et al., US Patent No. 4,901,234; claims 29-34 are rejected as being anticipated by Garde et al., US Patent No. 5,634,076; and claims 15 and 16 are rejected as being unpatentable over Heath et al., '234, in view of Kamiya, US Patent No. 5,809,335. In the present amendment, claims 2-4, 17-28, 30 and 35-37 have been canceled, and claims 1, 5-16, 29 and 31-34 have been amended.

As presently amended, the claims highlight a data transfer system and corresponding method having a direct memory access element including multiple data busses or interfaces, associated with multiple memories and or processors, and a plurality of node, which in at least some embodiments are associated with a plurality of peripherals. The direct memory access element is programmable and/or is adapted for configuring direct memory access data channels to enable the transfer of data between the plurality of nodes and one or more of the elements associated with the multiple interfaces and/or data busses. None of the references cited teach or suggest the use of a programmable and/or configurable direct memory access system, which provides reconfigurable direct access between at least three groupings of elements.

The applicants contend that the claims, as presently amended, are allowable over the prior art of record, for the reasons noted above. Allowance of the application is therefore respectfully requested. Should any issues remain unresolved after the consideration of the present response, the Examiner is invited to contact the applicant's representative at the number listed below to discuss the same.

Respectfully submitted,

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